## REMARKS

### Summary Of Office Action

Claims 1-33 are pending in the above-identified application.

The Examiner has rejected claims 1 and 2 under 35 U.S.C. § 102(b) as being anticipated by Yabe U.S. Patent No. 6,046,956. Claim 3 has been objected to as being dependent upon a rejected base claim, but allowable subject matter has been indicated. Claims 4-33 have been allowed.

### Summary Of Applicant's Reply

Applicant notes with appreciation the allowance of claims 4-33. Applicant also notes with appreciation the indication of allowable subject matter in claim 3, and hereby expressly reserves the right to rewrite claim 3 in independent form if its base claim is not ultimately allowed. The Examiner's rejection and objection are respectfully traversed.

### Applicant's Reply to the Prior Art Rejection

Claims 1 and 2 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Yabe. The Examiner's rejection is respectfully traversed.

Applicant's invention, as defined by independent claim 1, relates to a method of deactivating a word line in a memory circuit. The method includes activating a plurality of word lines, all the word lines being active concurrently, and deactivating one of the word lines, the other of the word lines remaining active. These features are illustrated in applicant's specification, which states, for example, in connection with FIG. 6:

> [T]he ACTIVE signal is pulsed three times in transitions 603-605 to activate all three WLs.

> Advantageously, however, the WLs can each be deactivated without asserting the PRE-CHARGE signal, and the deactivation of each WL need not be simultaneous with the deactivation of other WLs.

Page 7, lines 11-16. In contrast, Yabe relates to a semiconductor memory device having a plurality of memory cells arranged in a row/column array. Any particular word line can be activated to select a row in the array, while the other word lines remain inactive. For example, Yabe states that:

> In the WL boostless type DRAM as shown in FIGS. 2 and 3, the transfer gate T is driven, at an address selected time, by the power supply Vcc not boosted. And at the address not-selected time the word line WL is biased to the negative potential Vbb by the word line driver circuit 13.

Col. 2, lines 18-22. Thus, the word line driver circuit shown in FIG. 3 corresponds to a particular word line WL. The driver circuit activates WL if it is selected by address signals Xaj, XBk, and XCl. If WL is not selected by the address signals, the driver circuit will pull down WL to a deactivated state. Because the address signals XAj, XBk, and XCl can only select one word line at any given time, only one word line can be active at a particular time. Nowhere does Yabe show or suggest activating a plurality of word lines, all the word lines being active concurrently, as defined by applicant's claim 1. Accordingly, Yabe cannot show or suggest deactivating one of the activated word lines, the other of the word lines remaining active, as further defined by applicant's claim 1.

For at least the reasons set forth above, applicant respectfully submits that independent claim 1 is patentable. Accordingly, dependent claim 2 is also patentable. Applicant respectfully requests that the rejection to claims 1 and 2 be withdrawn.

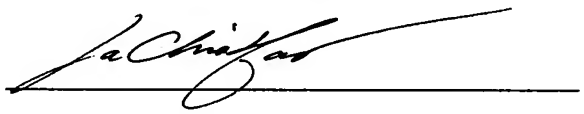
Applicants' Reply to the
Objection of Claim 3

For the reasons set forth above, applicant respectfully submits that independent claim 1 is patentable. Accordingly, dependent claim 3 should also be patentable. Applicant respectfully requests that the objection to claim 3 be withdrawn.

Conclusion

The foregoing demonstrates that claims 1-33 are patentable. Reconsideration and prompt allowance are respectfully requested.

Respectfully submitted,



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